PALM Intranet

Application Number Submit

IDS Flag Clearance for Application 10779817

IDS Information

Content	Mailroom Date	Entry Number	IDS Review	Last Modified	Reviewer
WIDS	2007-06-05	55	YE	2007-06-27 08:18:08.0	cbritt
WIDS	2007-02-27	42	Y	2007-05-09 00:00:00.0	CR #232884
WIDS	2004-07-29	40	Y	2007-05-09 00:00:00.0	CR #232884
WIDS	2006-03-21	34	Y	2007-05-09 00:00:00.0	CR #232884
WIDS	2004-09-28	29	Y	2007-05-09 00:00:00.0	CR #232884
Update					

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14627	(IC circuit (integrated adj circuit) chip) same (processing processor) same (error adj (detect detecting detector detected detection correct correcting correction corrected ECC EDC EDAC))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 15:59
L2	925	L1 and (repair repaired repairing fix)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 14:01
L3	177	L2 and (zero with error)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 14:01
L4	11	L3 and (dynamic\$ with (control controller controlling controlled) with (parameter variable))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 14:01
L5	521589	latch (flip adj flop) (scan adj element) flop	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 14:03
L6	1246993	delay (latch (flip adj flop) (scan adj element) flop)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 16:00
L7	272323	(IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 15:59
L8	101620	I6 and I7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 16:00
L9	17068	delay near3 ((latch (flip adj flop) (scan adj element) flop))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 16:00

L10	17	((nondelay non-delay non-delayed nondelayed) and (delayed delay)) near3 ((latch (flip adj flop) (scan adj element) flop)) and ((IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 16:03
L11	11	((nondelay non-delay non-delayed nondelayed) and (delayed delay)) near3 ((latch (flip adj flop) (scan adj element) flop)) and ((IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment)) and low adj power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 16:03
L12	11	((nondelay non-delay non-delayed nondelayed) and (delayed delay)) near3 ((latch (flip adj flop) (scan adj element) flop)) and ((IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment)) and (low adj power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 17:23
L14	0	((low adj power) and ((nondelay non-delay non-delayed nondelayed) and (delayed delay)) near3 ((latch (flip adj flop) (scan adj element) flop)) and ((IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment))).clm. and 714/724.ccls.	US-PGPUB	OR	ON	2007/06/27 17:26
L15	11	(low adj power) and (((nondelay non-delay non-delayed nondelayed) and (delayed delay)) near3 ((latch (flip adj flop) (scan adj element) flop))) and ((IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 17:26

S1	100	("5293389" "5596371" "5619261"	USPAT	OR	ON	2006/12/17 15:26
		"4593378" "4766506" "4809210"				
		"5285267" "5325495" "5333054"				
		"5627581" "5706402" "6144800"				
		"6209023" "4266146" "4443799"				
		"4466067" "4484270" "4782458"				
		"4897550" "4985131" "5020015"				
		"5191418" "5220424" "5302909"				
		"5315307" "5412436" "5663767"				
		"5717789" "5761370" "5881091"				
		"5898338" "5920357" "5949283"				
		"6005983" "6119527" "6185309"				
		"4270025" "4355333" "4403263" "4411246" "4464768" "4493036"				
		"4600992" "4604750" "4620799"			1	
		"4628461" "4628347" "4631575"				
		"4633516" "4767997" "4771470"				
		"4817058" "4829307" "4849826"				
		"4853336" "4858113" "4868650"		1		
		"4920507" "4951137" "5005419"				
		"5014271" "5204676" "5220683"				
		"5227866" "5233421" "5237625"				
		"5249037" "5251263" "5264486"				
		"5264745" "5289292" "5301331"				
		"5337089" "5339282" "5345311"				
		"5357331" "5361094" "5371548"				
		"5376924" "5383164" "5388266"				
		"5392070" "5424631" "5426433"				
		"5428764" "5432862" "5434426"				
		"5436882" "5444738" "5469214"				
		"5474078" "5499375" "5560020"				
		"5559972" "5559518" "5559517"				
		"5559516" "5559515" "5572338"				
		"5572591" ).pn.				
S2	2	"5553232".pn.	US-PGPUB;	OR	ON	2006/12/17 15:29
	_	,	USPAT;			,
			EPO; JPO;			
			DERWENT;			
			IBM TDB			
62	<b>a</b>	"E21262E" nn	_	OB	ON	2006/12/17 15:20
S3	2	"5313625".pn.	US-PGPUB; USPAT;	OR	ON	2006/12/17 15:30
			EPO; JPO;			
			DERWENT;			
			IBM_TDB			
			_			
S4	2	"5203003".pn.	US-PGPUB;	OR	ON	2006/12/17 15:30
			USPAT;			
			EPO; JPO;			
			DERWENT;			
			IBM_TDB			

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S5	2	"6188610".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/17 15:31
S6	1	"20010016927"	US-PGPUB	OR	ON	2006/12/17 15:31
S7	1	"20020038418"	US-PGPUB	OR	ON	2006/12/17 15:32
S8	1	"6476643".pn.	US-PGPUB; USPAT	OR	ON	2006/12/17 15:33
S9	1	"5615263".pn.	US-PGPUB; USPAT	OR	ON	2006/12/17 15:33
S10	1	"5627412".pn.	US-PGPUB; USPAT	OR	ON	2006/12/17 15:52
S11	5	"146800"	DERWENT	OR	ON	2006/12/17 15:53
S12	254	S1 S2 S3 I4I5 S6 S7 S8 S9 S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/17 15:54
S13	124	S1 S2 S3 I4I5 S6 S7 S8 S9 S10	USPAT	OR	ON	2007/01/06 12:07
S14	107	S1 S2 S3 S4 S5 S6 S7 S8 S9 S10	USPAT	OR	ON	2006/12/17 15:54
S15	2	"20040243893"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/06 13:41
S16	0	(10/779805).APP.	USPAT; USOCR	OR	ON	2007/01/06 12:23
S17	0	"7162661".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/06 12:23
S18	13939	(IC circuit (integrated adj circuit) chip) same (processing processor) same (error adj (detect detecting detector detected detection correct correcting correction corrected ECC EDC EDAC))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/06 13:44
S19	875	S18 and (repair repaired repairing fix)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/06 13:45

S20	162	S19 and (zero with error)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/06 13:45
S21	70	S20 and ((control controller controlling controlled) with (parameter variable))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/06 13:47
S22	10	S20 and (dynamic\$ with (control controller controlling controlled) with (parameter variable))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 15:51
S23	2	"2001175542"	JPO; DERWENT	OR	ON	2007/01/06 14:01
S24	1503	(delay delaying delayed) adj latch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:15
S25	834	(delay delaying delayed) adj latch and power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:15
S26	287	(delay delaying delayed) adj latch and ((low lower lowered less smaller) near3 power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:16
S27	82	(delay delaying delayed) adj latch and ((low lower lowered less smaller) near3 power) and capture	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:16
S28	73	(delay delaying delayed) adj latch and ((low lower lowered less smaller) near3 power) and capture and (processing processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:17
S29	18	(delay delaying delayed) adj latch and (((low lower lowered less smaller) near3 power) with (use usage consumption)) and capture and (processing processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/28 10:18

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S30	26	("20010016927" "20020038418" "390 5023" "5203003" "5313625" "5426746 " "5553232" "5615263" "5627412" "59 14903" "6188610" "6476643").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 15:50
S31	14455	(IC circuit (integrated adj circuit) chip) same (processing processor) same (error adj (detect detecting detector detected detection correct correcting correction corrected ECC EDC EDAC))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 15:51
S32	907	S31 and (repair repaired repairing fix)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 15:51
S33	174	S32 and (zero with error)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 15:51
S34	11	S33 and (dynamic\$ with (control controller controlling controlled) with (parameter variable))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/27 14:01
S35	11	(IC circuit (integrated adj circuit) chip) same (processing processor) same (error adj (detect detecting detector detected detection correct correcting correction corrected ECC EDC EDAC)) and (repair repaired repairing fix) and (zero with error) and (dynamic\$ with (control controller controlling controlled) with (parameter variable))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 15:53
S36	2	((IC circuit (integrated adj circuit) chip) same (processing processor) same (error adj (detect detecting detector detected detection correct correcting correction corrected ECC EDC EDAC)) and (repair repaired repairing fix) and (zero with error) and (dynamic\$ with (control controller controlling controlled) with (parameter variable))).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 16:12

6/27/07 5:27:35 PM C:\Documents and Settings\cbritt\My Documents\EAST\Workspaces\10392382.wsp

S37	2	((IC circuit (integrated adj circuit) chip) same (processing processor) same (error adj (detect detecting detector detected detection correct correcting correction corrected ECC EDC EDAC)) and (repair repaired repairing fix) and (zero with error) and (dynamic\$ with (control controller controlling controlled) with (parameter variable))).clm. and "714"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 16:13
S38	2	"7162661"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/12 16:13

# INTER FERENCE SEARCH

### **EAST Search History**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L16	7	((low adj power) and (((nondelay non-delay non-delayed nondelayed) and (delayed delay)) near3 ((latch (flip adj flop) (scan adj element) flop))) and ((IC circuit (integrated adj circuit) chip) same (processing processor) same (stage level block element segment))) and ("714"/\$.ccls. "365"/\$.ccls. "327"/\$.ccls. "324"/\$.ccls.)	US-PGPUB	OR	ON	2007/06/27 18:03

6/27/07 6:04:00 PM